

Appl. No. : 09/523,877
Filed : March 13, 2000

IN THE CLAIMS

Please amend Claims 37-40, 42, 43 and 53-63, and add new Claims 64-83 as follows:

1.-36 (Canceled)

5 37. (Currently amended) An extended and user-customized ~~configured pipelined~~ digital RISC processor having a pipeline, and an instruction set comprising a plurality of instructions comprising a base instruction set and at least one extension instruction, at least one of said base instruction set instructions or extension instructions comprising a branch instruction having a plurality of user-configurable modes determined by a plurality of bits
10 controlling the execution of at least one instruction in a delay slot following said branch instruction within said pipeline, each of said modes being constrained to only one of a plurality of unique combinations of said plurality of bits.

38. (Currently amended) An extended and user-customized ~~configured pipelined~~ digital RISC processor core having a pipeline, and an instruction set comprising a plurality of
15 instructions forming a base instruction set and at least one extension instruction, at least one of said instructions comprising a branch instruction including two data bits defining four discrete modes controlling the execution of at least one instruction in a delay slot following said branch instruction within said pipeline;

wherein said execution is controlled without regard to a branch direction metric.

20 39. (Currently amended) An extended ~~and user-configured pipelined~~ digital RISC processor having a pipeline and an instruction set, said processor comprising:

a user-customized processor core configuration rendered in a hardware description language model and including a base instruction set; and

at least one user-configured extension instruction within said instruction set, said at least
25 one extension instruction comprising a branch instruction having at least one mode controlling the execution of at least one instruction in a delay slot following said branch instruction within said pipeline using a plurality of data bits, at least one ~~of the~~ particular combination[s] of data bits and ~~the~~ a logical function[s] associated therewith being adapted for assignment by a user.

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40. (Currently amended) An extensible ~~and user-configurable pipelined~~ digital RISC processor design having a pipeline and base and extension instruction sets, at least one instruction within said base set comprising a branch instruction having four discrete modes for controlling the execution of at least one instruction in a delay slot following said branch

5 instruction within said pipeline, said processor design comprising:

a user-customized processor core configuration rendered in a hardware description language model and including said base instruction set; and

at least one user-customized extension instruction within said extension instruction set; wherein each of said modes provides unique functionality with respect to the other three

10 modes.

41. (Cancelled)

42. (Currently amended) The digital processor of Claim 40, wherein first and second of said ~~at least~~ four modes implement one- and two-cycle stalls within said pipeline, respectively.

15 43. (Currently amended) The digital processor of Claim 42, wherein at least one of said ~~at least~~ four modes operates without respect to a branch displacement metric.

44.-52. (Cancelled)

53. (Currently amended) The processor of Claim 37, wherein said bits are encoded in said branch instruction, and said bits of said branch instruction comprise two data bits
20 defining four discrete modes controlling said execution, said execution further being controlled without regard to a branch direction metric.

54. (Currently amended) The processor of Claim 37, wherein said bits are encoded in said branch instruction, and at least one of ~~the particular~~ said unique combinations of said bits of said branch instruction and ~~the~~ a logical function[s] associated therewith are adapted for
25 assignment by a user.

55. (Currently amended) The processor of Claim 53, wherein at least one of ~~the particular~~ said unique combinations of said bits of said branch instruction and ~~the~~ a logical function[s] associated therewith are adapted for assignment by a user.

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56. (Currently amended) The processor of Claim 38, wherein each of said four discrete modes is constrained to only one of a plurality of unique combinations of said ~~plurality~~ of two bits.

57. (Currently amended) The processor of Claim 38, wherein said bits are encoded in said branch instruction, and at least one of ~~the particular~~ said unique combinations of said bits of said branch instruction and ~~the~~ a logical function[s] associated therewith are adapted for assignment by a user.

58. (Currently amended) The processor of Claim 56, wherein said bits are encoded in said branch instruction, and at least one of ~~the particular~~ said combinations of said bits of said branch instruction and ~~the~~ a logical functions associated therewith are adapted for assignment by a user.

59. (Currently amended) ~~An extended and user-configured digital RISC processor~~
A user-customized and user-extended RISC processor core having at least one pipeline comprising at least instruction fetch, decode, and execute stages, and an associated data storage device, wherein the execution of instructions within said at least one pipeline is controlled by the method comprising:

storing an instruction set within said data storage device, said instruction set comprising a plurality of instruction words, each of said instruction words comprising a plurality of data bits, at least one of said instruction words comprising a user-configurable branch instruction having a plurality of unique functional modes exclusively associated with respective ones of unique combinations of a plurality of mode control bits, said branch instruction directing branching to a first address within said data storage device;

assigning one of a plurality of values to each of said mode control bits of said at least one branch instruction;

decoding said at least one branch instruction including said assigned values;

determining whether to execute an instruction within said pipeline in a stage preceding that of said at least one branch instruction based at least in part on said assigned values;

branching to said first address based on said at least one branching instruction; and

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performing, based at least in part on said act of decoding said assigned values, at least one other function dictated by the unique functional mode associated with said assigned values; wherein said processor core has a configuration determined at least in part by said user-customization and user-extension at the time of its design.

5 60. (Currently amended) A method of controlling the execution of instructions within an extended and user-customized configured pipelined RISC processor having a pipeline, said processor further being generated from a hardware description language model, comprising:

providing, as part of said description language model, an instruction set comprising a plurality of instruction words, each of said instruction words comprising a plurality of data bits, at least one of said words comprising a jump instruction having at least one user-configurable mode and at least one user-definable mode associated therewith, said user-configurable and user-definable modes each being specified by the same ones of said plurality of data bits, said at least one user-definable mode not being predetermined in terms of function;

10 assigning one of a plurality of values to said ones of said data bits of said at least one jump instruction; and

15 controlling the execution of at least one subsequent instruction within said pipeline based on said one assigned value of said ones of data bits when said at least one jump instruction is decoded;

20 wherein said method further comprises generating a long immediate constant using a single word instruction by:

providing an instruction word having an op-code and at least one short immediate value associated therewith, said at least one short immediate value comprising a plurality of bits;

25 selecting a portion of said plurality of bits of said at least one short immediate value;

shifting all of said bits of said at least one short immediate value using said op-code and only said portion of bits to produce a shifted immediate value; and

storing said shifted immediate value in a register.

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61. (Currently amended) A method of controlling the execution of instructions within an extended and user-customized ~~configured~~ ~~pipelined~~ RISC processor having a pipeline, said processor further being generated from a hardware description language model, comprising:

providing, as part of said description language model, an instruction set comprising a plurality of instruction words, each of said instruction words comprising a plurality of data bits, at least one of said words comprising a jump instruction having at least one user-configurable mode and at least one user-definable mode associated therewith, said user-configurable and user-definable modes each being specified by the same ones of said plurality of data bits, said at least one user-definable mode not being predetermined in terms of function;

assigning one of a plurality of values to said ones of said data bits of said at least one jump instruction; and

controlling the execution of at least one subsequent instruction within said pipeline based on said one assigned value of said ones of data bits when said at least one jump instruction is decoded; and

wherein at least one of said plurality of instruction words comprises an op-code, a plurality of fields each comprising a plurality of bits, and at least one short immediate value comprising a plurality of bits, said at least one instruction word being encoded according to the method comprising:

associating a first of said fields with a first data source;

associating a second of said fields with a second data source; and

performing a logical operation using said first and second data sources as operands, said logical operation being specified by said op-code;

wherein said at least one instruction word is used to generate a long immediate constant according to the method comprising:

selecting a portion of said plurality of bits of said at least one short immediate value;

shifting all of said bits of said at least one short immediate value using said op-code and only said portion of bits to produce a shifted immediate value; and

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storing said shifted immediate value in a register.

62. (Currently amended) ~~A user-configured and~~ An extended RISC processor comprising:

a user-customized processor core having a multistage instruction pipeline, said core
5 being adapted to decode and execute instruction words;

a data interface between said processor core and an information storage device; and

an instruction set comprising a plurality of said instruction words, at least one of said instruction words being a user-configurable jump instruction containing data defining a plurality of jump delay slot modes and at least one user-defined mode, said jump delay slot modes and at
10 least one user-defined mode each being specified by the same portions of said data, said at least one user-defined mode not being predetermined in terms of function, said plurality of modes controlling the execution of instructions within said instruction pipeline of said processor core in response to said at least one jump instruction word within said instruction set;

wherein said processor is further adapted to generate a long immediate constant using a
15 single word instruction by:

providing an instruction word having an op-code and at least one short immediate value associated therewith, said at least one short immediate value comprising a plurality of bits;

selecting a portion of said plurality of bits of said at least one short immediate
20 value;

shifting all of said bits of said at least one short immediate value using said op-code and only said portion of bits to produce a shifted immediate value; and storing said shifted immediate value in a register.

63. (Currently amended) ~~A user-configured and~~ An extended digital processor
25 comprising:

a user-customized processor core having a multistage instruction pipeline, said core being adapted to decode and execute instruction words;

a data interface between said processor core and an information storage device; and

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an instruction set comprising a plurality of said instruction words, at least one of said instruction words being a user-configurable jump instruction containing data defining a plurality of jump delay slot modes and at least one user-defined mode, said jump delay slot modes and at least one user-defined mode each being specified by the same portions of said data, said at least one user-defined mode not being predetermined in terms of function, said plurality of modes controlling the execution of instructions within said instruction pipeline of said processor core in response to said at least one jump instruction word within said instruction set;

wherein said at least one of said plurality of instruction words comprises an op-code, a plurality of fields each comprising a plurality of bits, and at least one short immediate value comprising a plurality of bits, said at least one instruction word being encoded by:

associating a first of said fields with a first data source;

associating a second of said fields with a second data source; and

performing a logical operation using said first and second data sources as operands, said logical operation being specified by said op-code; and

wherein said at least one instruction word is used to generate a long immediate constant ~~by according to the method comprising:~~

selecting a portion of said plurality of bits of said at least one short immediate value;

shifting all of said bits of said at least one short immediate value using said op-code and only said portion of bits to produce a shifted immediate value; and

storing said shifted immediate value in a register.

64. (New) An extended and user-customized digital RISC processor core having a pipeline, and an instruction set comprising a plurality of instructions comprising a base instruction set and at least one extension instruction, at least one of said base instruction set instructions or extension instructions comprising a branch instruction having a plurality of user-configurable modes determined by a plurality of bits controlling the execution of at least one instruction in a delay slot following said branch instruction within said pipeline, each of said

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modes being constrained to only one of a plurality of unique combinations of said plurality of bits;

wherein said core is user-customized at time of its design.

65. (New) An extended and user-customized digital RISC processor having a
5 pipeline, and an instruction set comprising a plurality of instructions forming a base instruction set and at least one extension instruction, at least one of said instructions comprising a branch instruction including two data bits defining four discrete modes controlling the execution of at least one instruction in a delay slot following said branch instruction within said pipeline;

wherein said execution is controlled without regard to a branch direction metric; and

10 wherein said processor is user-customized at time of its design.

66. (New) An extended and user-customized digital RISC processor having a pipeline and an instruction set, said processor comprising:

a processor core configuration including a base instruction set; and

15 at least one user-configured extension instruction within said instruction set, said at least one extension instruction comprising a branch instruction having at least one mode controlling the execution of at least one instruction in a delay slot following said branch instruction within said pipeline using a plurality of data bits, at least one particular combination of data bits and a logical function associated therewith being adapted for assignment by a user;

wherein said core is user-customized at time of its design..

20 67. (New) An extensible and user-customizable digital RISC processor design having a pipeline and base and extension instruction sets, at least one instruction within said base set comprising a branch instruction having four discrete modes for controlling the execution of at least one instruction in a delay slot following said branch instruction within said pipeline, said processor design comprising:

25 a processor core configuration including said base instruction set; and

at least one user-customized extension instruction within said extension instruction set;

wherein each of said modes provides unique functionality with respect to the other three modes; and

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wherein said core is user-customized at time of its design.

68. (New) An extended and user-customized digital RISC processor core having a pipeline, and an instruction set comprising a plurality of instructions comprising a base instruction set and at least one extension instruction, at least one of said base instruction set
5 instructions or extension instructions comprising a branch instruction having a plurality of user-configurable modes determined by a plurality of bits controlling the execution of at least one instruction in a delay slot following said branch instruction within said pipeline, each of said modes being constrained to only one of a plurality of unique combinations of said plurality of bits;

10 wherein said processor core is user-customized by at least:

receiving one or more inputs from a user for at least one customized parameter of said processor; and

generating through an automated process a customized description language model of said core based on the least one customized parameter.

15 69. (New) The processor core of Claim 68, wherein said automated process comprises modifying at least one prototype description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter.

70. (New) The processor core of Claim 68, wherein said processor core is further
20 user-customized by generating, through an automated process, test code associated with the customized description language model based on the at least one customized parameter; and

71. (New) The processor core of Claim 68, wherein the customized description language model includes both functional and structural description language descriptions for the processor core.

25 72. (New) An extended and user-customized digital RISC processor core having a pipeline, and an instruction set comprising a plurality of instructions forming a base instruction set and at least one extension instruction, at least one of said instructions comprising a branch

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instruction including two data bits defining four discrete modes controlling the execution of at least one instruction in a delay slot following said branch instruction within said pipeline;

wherein said execution is controlled without regard to a branch direction metric; and

wherein said processor core is user-customized by at least:

5 receiving one or more inputs from a user for at least one customized parameter of said processor; and

generating through an automated process a customized description language model of said core based on the least one customized parameter.

73. (New) The processor core of Claim 72, wherein said automated process
10 comprises modifying at least one prototype description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter.

74. (New) The processor core of Claim 72, wherein said processor core is further
15 user-customized by generating, through an automated process, test code associated with the customized description language model based on the at least one customized parameter; and

75. (New) The processor core of Claim 72, wherein the customized description
language model includes both functional and structural description language descriptions for the processor core.

76. (New) An extended and user-customized digital RISC processor having a
20 pipeline and an instruction set, said processor comprising:

a processor core configuration including a base instruction set; and

at least one user-configured extension instruction within said instruction set, said at least
one extension instruction comprising a branch instruction having at least one mode controlling
the execution of at least one instruction in a delay slot following said branch instruction within
25 said pipeline using a plurality of data bits, at least one particular combination of data bits and a
logical function associated therewith being adapted for assignment by a user;

wherein said processor core configuration is user-customized by at least:

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receiving one or more inputs from a user for at least one customized parameter of said processor; and

generating through an automated process a customized description language model of said core based on the least one customized parameter.

5 77. (New) The processor of Claim 76, wherein said automated process comprises modifying at least one prototype description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter.

78. (New) The processor of Claim 76, wherein said processor core is further user-customized by generating, through an automated process, test code associated with the
10 customized description language model based on the at least one customized parameter; and

79. (New) The processor of Claim 76, wherein the customized description language model includes both functional and structural description language descriptions for the processor core.

80. (New) An extensible and user-customizable digital RISC processor design
15 having a pipeline and base and extension instruction sets, at least one instruction within said base set comprising a branch instruction having four discrete modes for controlling the execution of at least one instruction in a delay slot following said branch instruction within said pipeline, said processor design comprising:

a processor core configuration including said base instruction set; and
20 at least one user-customized extension instruction within said extension instruction set; wherein each of said modes provides unique functionality with respect to the other three modes;

wherein said processor core configuration is user-customized by at least:

receiving one or more inputs from a user for at least one customized parameter
25 of said processor; and

generating through an automated process a customized description language model of said core configuration based on the least one customized parameter.

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81. (New) The processor design of Claim 80, wherein said automated process comprises modifying at least one prototype description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter.

5 82. (New) The processor design of Claim 80, wherein said processor core configuration is further user-customized by generating, through an automated process, test code associated with the customized description language model based on the at least one customized parameter; and

10 83. (New) The processor design of Claim 80, wherein the customized description language model includes both functional and structural description language descriptions for the processor core configuration.